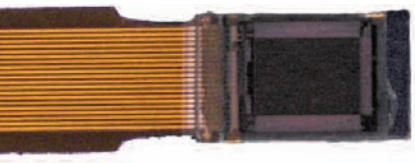
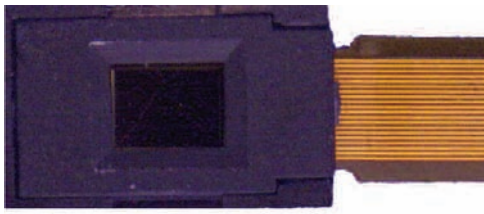
# CyberDisplay® 230K LV

## Low-Voltage, Ultra-Compact Color QVGA AMLCD



***Frameless***
Part No. KCD-QDNF-AA

***Framed***
Part No. KCD-QDNF-BA



## 1 GENERAL DESCRIPTION

The CyberDisplay® 230K LV is a color-filter active matrix liquid crystal display (AMLCD) with a spatial resolution of 320 x 240 (QVGA). The CyberDisplay 230K LV utilizes high-performance single-crystal silicon transistors and is the smallest (0.24 inch diagonal) transmissive AMLCD for QVGA resolution. The transmissive AMLCD allows the use of simple and thin optics for compact size.

The CyberDisplay 230K LV features Kopin's patent-pending low-voltage architecture for low power consumption and compatibility with CMOS driver ICs. The input video levels are reduced to half the typical values for other LCDs because the capacitively coupled interface effectively doubles the voltage written to pixels while the integrated switch circuitry restores the DC level. Bidirectional horizontal and vertical scanner circuits are integrated. A sleep mode is provided to facilitate and simplify system power management schemes.

Figure 1-1 shows the pixel array layout. Each square full-color pixel is composed of three primary color dots. The active array of 960 × 240 dots is surrounded by opaque dummy pixels for a total array size of 972 × 244 dots.

The CyberDisplay 230K LV is available in a frameless package (KCD-QDNF-AA) for integration into a viewfinder module or a framed package (KCD-QDNF-BA) for attachment to a snap-on backlight module.

### *1.1 Applications*

The ultra-compact CyberDisplay 230K LV is ideal for viewfinders for digital cameras or lightweight eyewear for watching movies, sporting events and music videos, browsing the Web and checking e-mail from mobile devices such as cell phones, or playing games on the go.

### *1.2 Key Specifications*

- 320 × 3 × 240 active color dots (QVGA resolution)
- 324 × 3 × 244 total color dots
- 5 (W) × 15 (H) µm dot pitch
  (15 × 15 µm square color pixels)
- Ultra-compact 0.24"-diagonal
- Active pixel area (4.8 mm × 3.6 mm)
- Parallel RGB analog input
- Simple 3.3-volt interface for CMOS compatible driver chip
- Power-saving sleep mode
- Integrated horizontal and vertical scanners
- Bidirectional horizontal and vertical scanning

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# 2 ELECTRICAL SPECIFICATIONS

A block diagram showing inputs, outputs, and functions is shown in Figure 2-1.

External capacitors couple the RGB component signals to the display's six video inputs, with one pair of high and low inputs for each primary color (red, green, and blue).

The row inversion drive scheme requires that video polarity be inverted on alternating rows, with the INV signal selecting the high or low inputs.

Integrated scanners drive the active matrix pixel array. The horizontal and vertical scan directions are controlled by the RGT and DWN inputs, respectively.

## *2.1 Interface signals*

A 20-pin flex cable provides the electrical connection to the CyberDisplay 230K. Interface signals are listed in Table 2-1.

## *2.2 Inversion*

To preserve DC balance in the liquid crystal, each pixel must be driven with alternating high and low video. The CyberDisplay 230K LV uses row inversion, in which all pixels of each row have the same polarity, but successive rows have alternating polarity. The INV signal indicates the polarity of each row (see timing diagrams of Section 2.5). The row inversion phases must

| Pin | Symbol | Description |
|---|---|---|
| 1 | VEE | Supply = 0V |
| 2 | VIDRH | High red video input |
| 3 | VIDGH | High green video input |
| 4 | VIDBH | High blue video input |
| 5 | VIDRL | Low red video input |
| 6 | VIDGL | Low green video input |
| 7 | VIDBL | Low blue video input |
| 8 | HS | Horizontal sync |
| 9 | VS | Vertical sync |
| 10 | INV | Inversion polarity |
| 11 | DWN | Vertical scan direction (H = top-to-bottom) |
| 12 | RGT | Horizontal scan direction (H = left-to-right) |
| 13 | SLEEP* | Sleep mode |
| 14 | CK0 | Clock |
| 15 | CK1 | Clock |
| 16 | VDD | Supply |
| 17 | VSS | Supply = –5V |
| 18 | TOUT1 | Test output |
| 19 | TOUT2 | Test output |
| 20 | VEE | Supply = 0V |

* Signal is active low

**Table 2-1:** Interface Pin List

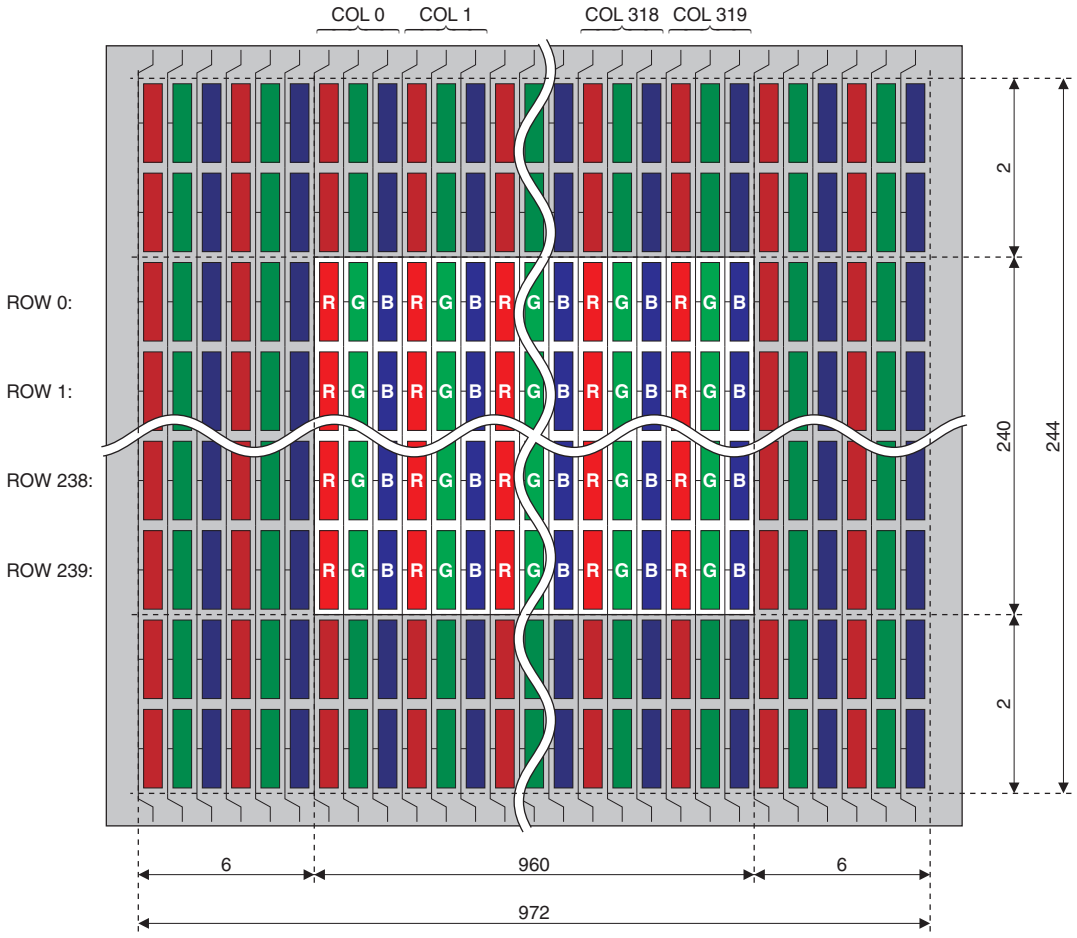


**Figure 1-1:** Pixel Array.

be inverted with successive fields. For example, if one field is driven with row 0 low, row 1 high, and row 2 low, then the following field must have row 0 high, row 1 low, and row 2 high.

### *2.3 Sleep mode*

The CyberDisplay 230K LV features a sleep mode to simplify system power management. When the SLEEP* pin is driven low, all scanners are disabled and the pixel array is driven to the white state. The display may remain powered and will draw minimal current while in sleep mode. The backlight may be turned off.

The display will also enter sleep mode when the integrated low voltage detect circuit determines that power has been removed.

### *2.4 Electrical characteristics*

Permanent damage to the display may result if the Absolute Maximum Ratings in Table 2-2 are exceeded. The Absolute Maximum Ratings are not typical operating conditions. Table 2-3 shows electrical characteristics and Recommended DC Operating Conditions.

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Supply voltage — source | $V_{DD}$ | – 0.5 | 5 | V |
| Supply voltage — sink | $V_{SS}$ | – 7.0 | 0.5 | V |
| All inputs | $V_I$ | $V_{SS}$– 0.5 | $V_{DD}$+ 0.5 | V |

**Table 2-2: Absolute Maximum Ratings**
Note: All voltages relative to $V_{EE}$=0

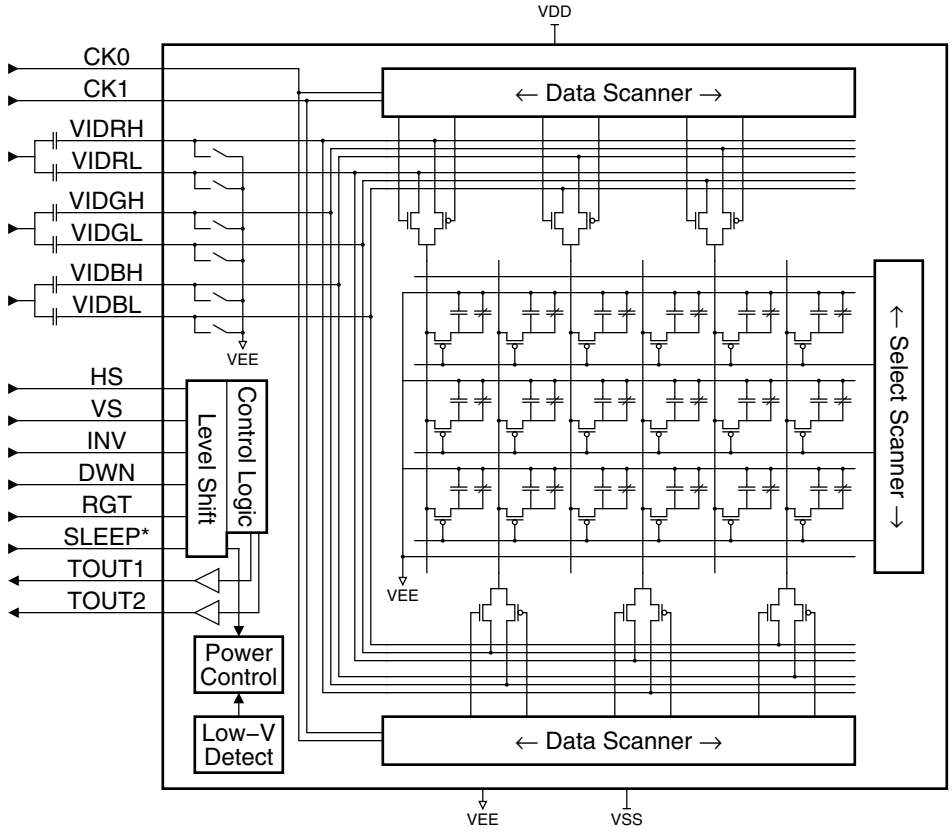


**Figure 2-1:** Block Diagram

**Table 2-3** Electrical Characteristics (Note: All voltages relative to $V_{EE}$=0)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply voltage — source | VDD | 3 | 3.5 | 3.6 | V |
| Supply voltage — sink | VSS | – 5.5 | – 5.0 | – 4.5 | V |
| Operating current — source | IDD | | 0.4 | | mA |
| Operating current — sink | ISS | | 0.4 | | mA |
| Operating current | IEE | – 100 | | 100 | µA |
| VID[RGB]H high black level | VHK | | 3.3 | | V |
| VID[RGB]H high white level | VHW | | 0 | | V |
| VID[RGB]L low white level | VLW | | 0 | | V |
| VID[RGB]L low black level | VLK | | – 3.3 | | V |
| Digital input high | VIH | 0.9 VDD | | | V |
| Digital input low | VIL | | | 0.1 VDD | V |
| Input current | II | – 10 | | 10 | µA |
| Input capacitance: video inputs | CVID | | 22 | 27 | pF |
| Input capacitance: CK0 & CK1 | CC | | 12 | 18 | pF |
| Input capacitance: other inputs | CI | | 5 | 10 | pF |

### *2.5 Timing specification*

The parameters shown in Table 2-4 are defined in the timing diagrams, Figures 2-2 through 2-5, which follow.

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Field period | $t_v$ | | 16.7–20.0 | | ms |
| Field rate | $1/t_v$ | | 50–60 | | Hz |
| Line period | $t_h$ | | 64 | | µs |
| Line rate | $1/t_h$ | | 15.6–15.7 | | kHz |
| Clock period | $t_{cp}$ | 300 | 325 | 1000 | ns |
| HS high pulse width | $t_{hh}$ | 5 | | | µs |
| HS to CK0 pulse 0 delay | $t_{fd}$ | 1 | | | µs |
| CK1 pulse 327 to HS delay | $t_{bd}$ | 1 | | | µs |
| Clock high pulse width | $t_{ch}$ | 100 | | | ns |
| CK0 to CK1 delay | $t_{cd}$ | $(t_{cp}/2)–5$ | $t_{cp}/2$ | $(t_{cp}/2)+5$ | ns |
| CK0 and CK1 non-overlap | $t_{nol}$ | 0 | 5 | | ns |
| White hold after HS | $t_{wh}$ | 400 | | | ns |
| White setup before HS | $t_{ws}$ | 200 | | | ns |
| Video setup | $t_{vs}$ | 80 | | | ns |
| Video hold | $t_{vh}$ | 50 | | | ns |
| INV setup before HS | $t_{is}$ | 100 | | | ns |
| INV hold after HS | tih | 100 | | | ns |
| VS high pulse width | $t_{vsh}$ | 1 | | | µs |
| VS low pulse width | $t_{vsl}$ | 1 | | | µs |
| VS to HS delay | $t_{vhd}$ | 1 | | | µs |
| HS to VS delay | $t_{hvd}$ | 1 | | | µs |

**Table 2-4:** Electrical Characteristics and Recommended AC Operating Conditions

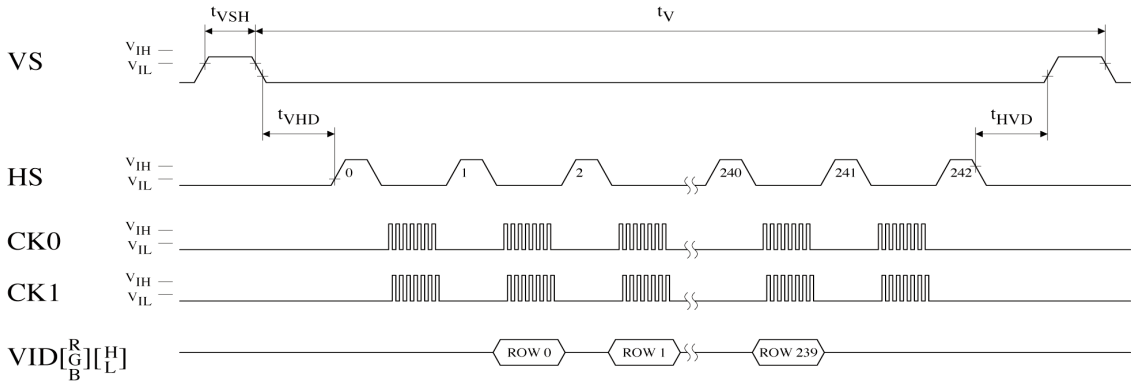


**Figure 2-2:** Vertical Timing, Top-to-Bottom Scan

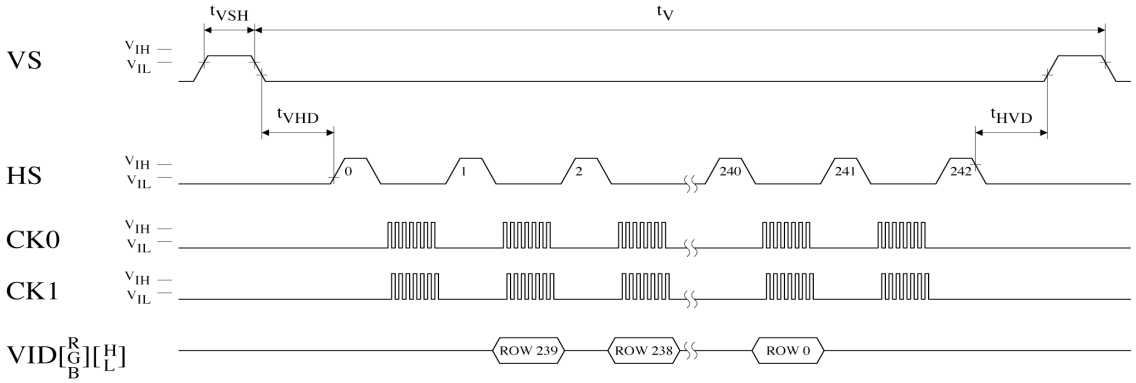


**Figure 2-3:** Vertical Timing, Bottom-to-Top Scan

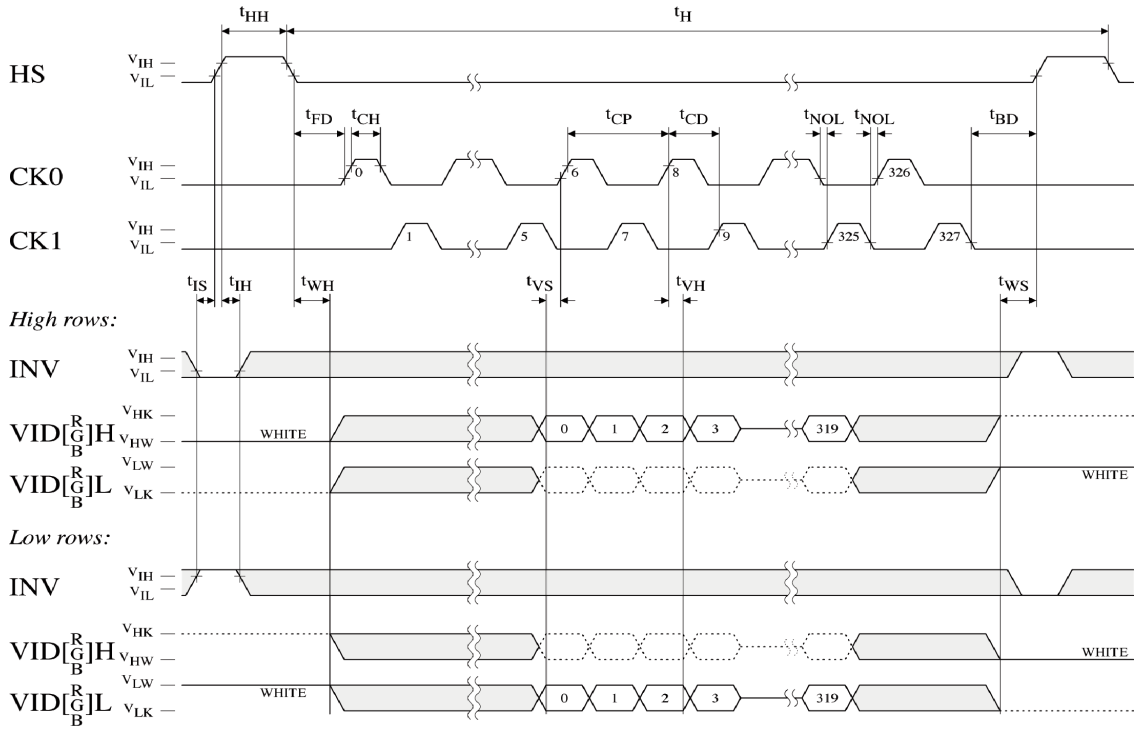


**Figure 2-4:** Horizontal Timing, Left-to-Right Scan

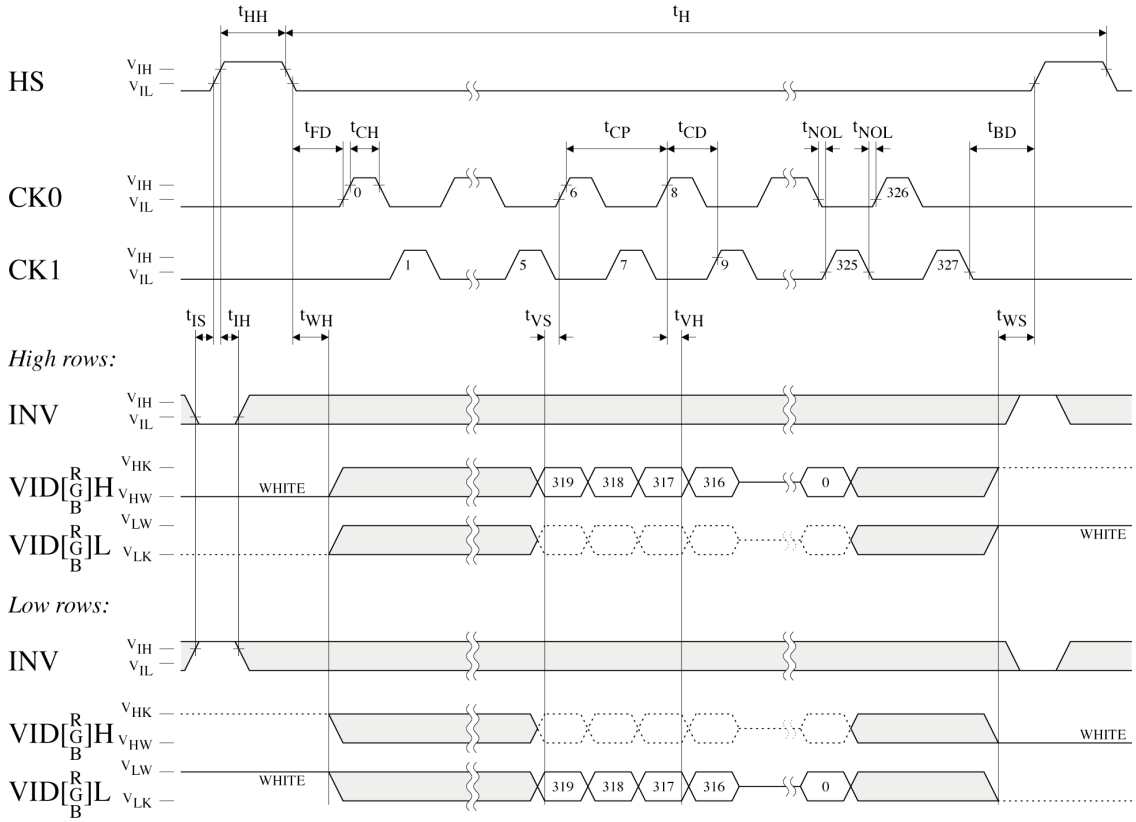


**Figure 2-5:** Horizontal Timing, Right-to-Left Scan

### *2.6 Line skipping*

Simple vertical scaling may be accomplished by line skipping. For example, to display PAL video with the correct aspect ratio, one of every six lines should be skipped. As illustrated in Figure 2-6, the HS pulse should be extended to remain high during the skipped line. This technique mimimizes visible artifacts by preserving the same HS-video timing in the rows before and after the skipped line.

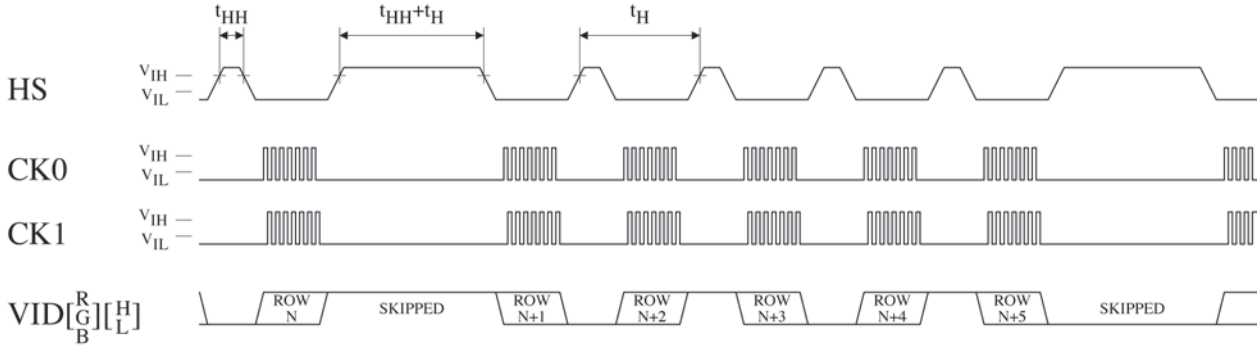


**Figure 2-6:** Line Skipping Timing Diagram

# 4 MECHANICAL SPECIFICATIONS

## *4.1 Interconnect*

The flexible PC cable is strain relieved, but tugging forces should be limited to less than 0.5 kg perpendicular to the display and less than 1 kg parallel to the display. The minimum inside bend radius for the cable is .03 inches. Repeated reformings are not recommended.

## *4.2 Mechanical drawings*

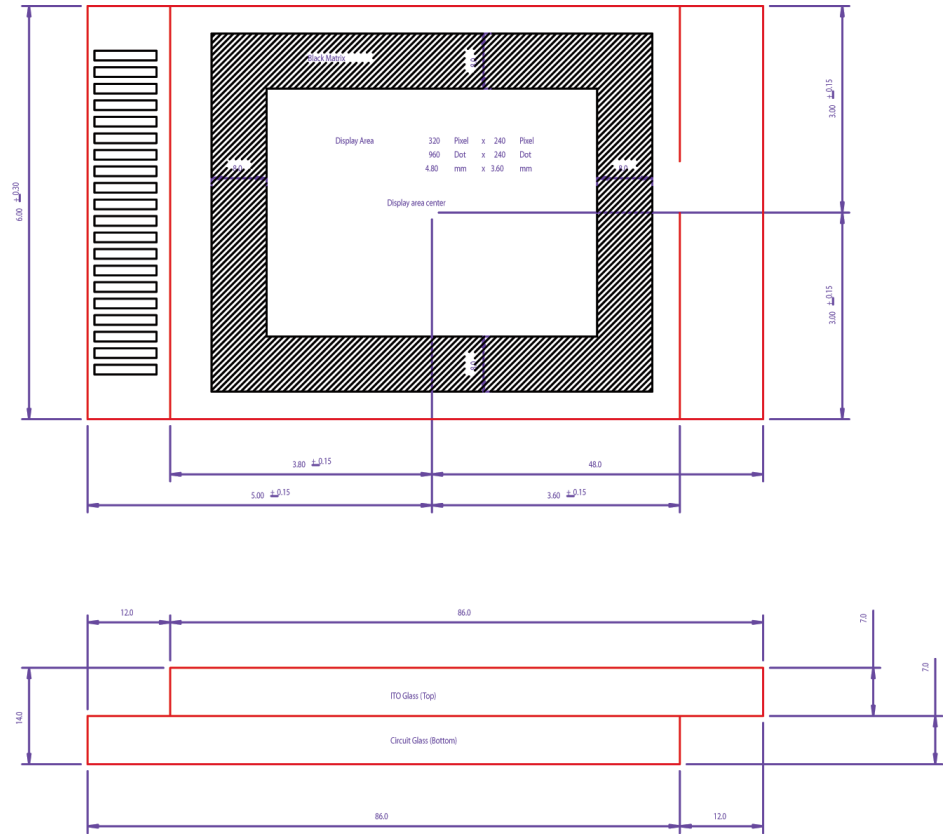


**Figure 4-1:** CyberDisplay 230K LV Display and Pixel Array Area

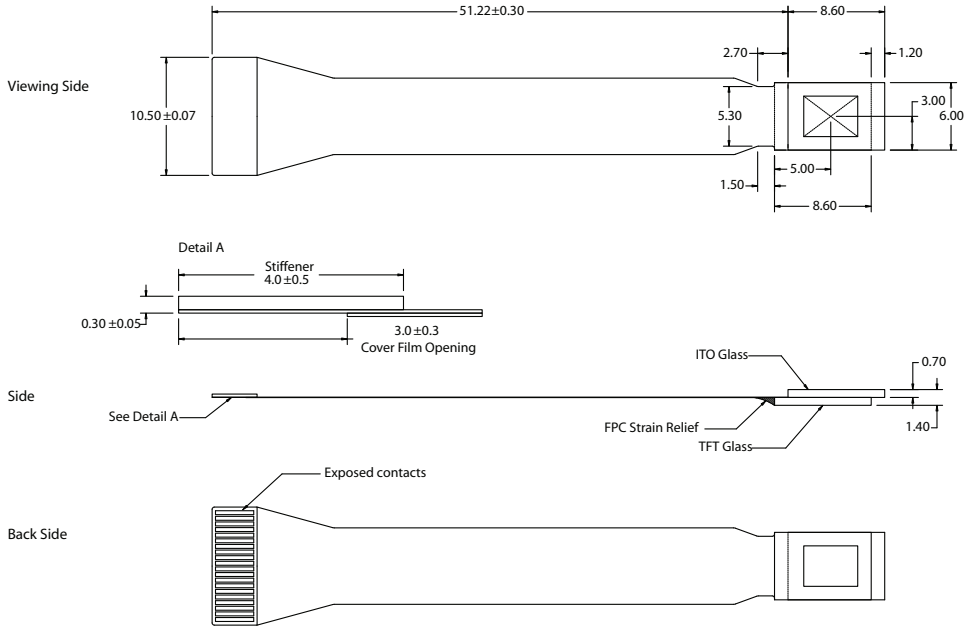


**Figure 4-2:** CyberDisplay 230K LV Display (frameless)

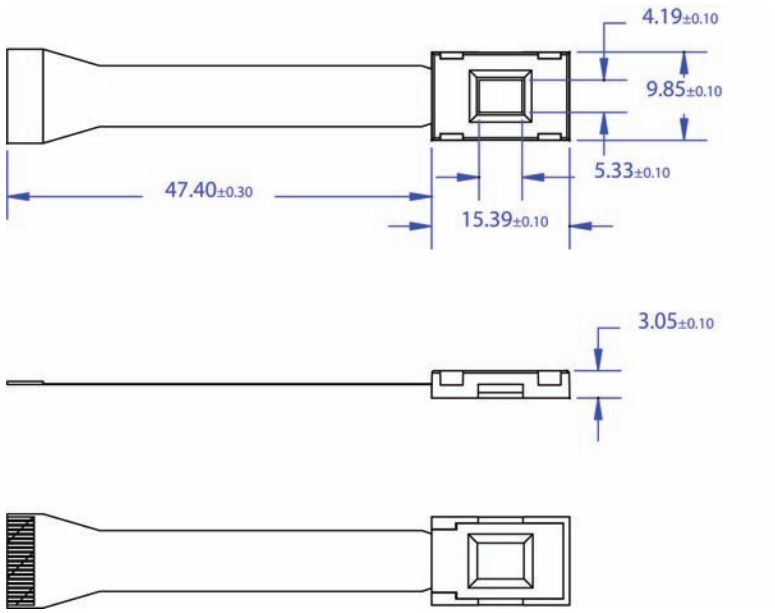


**Figure 4-3:** CyberDisplay 230K LV Display and FPC Assembly (framed)