

# A New Drive-Scheme Architecture for AMLCDs Used in Microdisplays

*The development of a new ac-coupled architecture will allow compact low-power near-to-eye microdisplays to operate by using CMOS-compatible 3.3-V power supplies.*

by Alan Richard and Frederick P. Herrmann

**A**S video-on-the-go becomes a new and important application, there is an increasing need for low-power high-resolution near-to-eye microdisplays that will bring large images to portable devices for consumer applications such as watching movies, music videos, and live television.

One obvious way to reduce power consumption is to lower the operating voltage. However, it has been difficult to lower the operating voltage of displays, particularly liquid-crystal displays (LCDs) because the display contrast tends to improve with higher drive voltage. The higher voltage is also an impediment in reducing system cost because LCD driver chips often require more-expensive BiCMOS processes that satisfy display drive requirements.

A newly developed architecture for active-matrix LCDs (AMLCDs) reduces the interface signal levels, making them compatible with conventional CMOS technology. The drive scheme effectively doubles the voltage written to the pixels by using external coupling capacitors and dc-restore switches integrated into the display, without switching the voltage of the common electrode (VCOM). Instead, the VCOM is held at a fixed dc level, 0 V in this implementation.

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The drive scheme is supported by low-cost CMOS driver chips for color and monochrome applications. The drivers feature charge pumps that allow the entire display system to be powered from a single 3.3-V power supply.

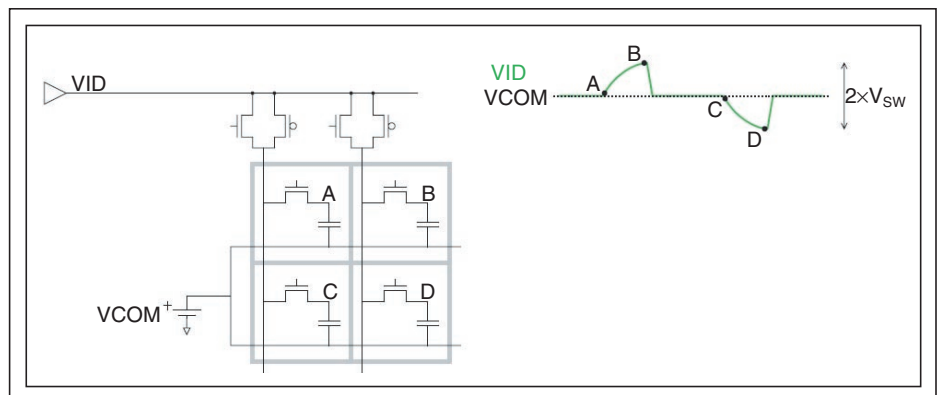
## Conventional Drive Schemes

It is well-known that liquid crystals do not operate well when powered by dc voltages. A dc bias across an LC cell will cause charge to accumulate on the cell plates, resulting in short-term image retention and/or possible long-term damage. The customary solution is to periodically invert the drive voltage in time (frame by frame) and space (row by row). For example, in a conventional twisted-nematic

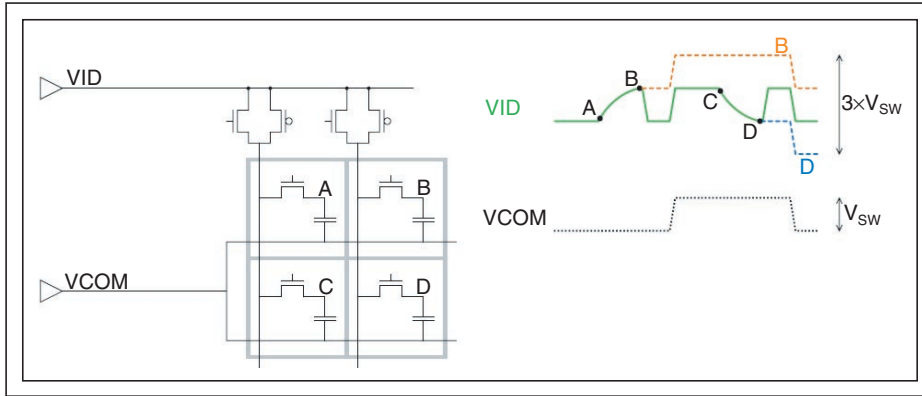
(TN) cell configuration, the pixels will darken in response to a voltage that is either positive or negative with respect to the common electrode. To preserve zero dc bias, positive video can be used for the even rows and negative video for the odd rows of one frame, with the polarity inverted for each successive frame.

For the conventional “dc common” drive scheme in which the common electrode is held at a dc level (VCOM), the external amplifier drives the video signal which is centered at VCOM and swings  $\pm V_{SW}$  to the high and low black levels (Fig. 1). Complementary pairs of NMOS and PMOS transistors switch the video onto the columns.

In the simplified four-pixel display shown in Fig. 1, pixel A is written first. The column



**Fig. 1:** For the conventional dc-common display architecture, the external amplifier drives the video signal, which is centered at VCOM and swings  $\pm V_{SW}$  to the high and low black levels. Complementary pairs of NMOS and PMOS transistors switch the video onto the columns.



**Fig. 2:** The conventional ac-common drive scheme can reduce the amplifier swing to  $1 \times V_{SW}$  over the frame time if the common electrode voltage is driven with a square wave of amplitude  $1 \times V_{SW}$ .

drivers sample the video line at the VCOM level, thus producing a white pixel. The second column is sampled when the video is at the  $V_{COM} + V_{SW}$  level, thereby driving pixel B to black. Negative video is used for the second row, making pixel C white at VCOM and pixel D black at  $V_{COM} - V_{SW}$ . For the dc-common scheme, the amplifier swing is only  $1 \times V_{SW}$  during any row time, but the total swing over the frame time is  $2 \times V_{SW}$ .

Alternatively, the “ac-common” drive scheme can reduce the amplifier swing to  $1 \times V_{SW}$  over the frame time if the common electrode voltage is driven with a square wave of amplitude  $1 \times V_{SW}$  (Fig. 2). As in the dc-common case, low and high voltages (white and black) are written to pixels A and B of the first row. Before row 2 is written, however, VCOM is increased by  $V_{SW}$ . Then, a high voltage written to pixel C results in 0 V across the cell and puts it in a white state and a low voltage written to pixel D puts it in a black state ( $-V_{SW}$ ).

However, toggling the common electrode in this manner affects not only the active row, but all of the pixels in the array. For example, when VCOM is high, pixel B is coupled up by

an additional  $V_{SW}$  to  $2 \times V_{SW}$ . Similarly, pixel D will be coupled down to  $-V_{SW}$  on the falling edge of VCOM. The maximum swing for the entire pixel array is therefore  $3 \times V_{SW}$ , compared to only  $2 \times V_{SW}$  for a dc-common scheme. Thus, for the ac-common scheme, a large pixel swing is more demanding on the display’s circuits because the pixel transistors and row drivers, which are not shown in the figure, must be designed to keep the inactive pixels turned off across a greater voltage range.

### ac-Coupled Drive

The new drive is built on an ac-coupled architecture that combines the advantages of the dc- and ac-common drive schemes (Table 1). This approach reduces the amplifier swing to  $1 \times V_{SW}$ , as in the ac-common case, without increasing the pixel voltage swing or requiring a VCOM driver. In fact, VCOM can be simply tied to ground.

In the new structure, a single amplifier drives the VID signal with a swing of  $1 \times V_{SW}$  (Fig. 3). Two external capacitors couple the VID signal to the display input signals VIDH and VIDL. The first capacitor

ideally has 0 V across it, making VIDH equal to VID. However, the dc voltage on the second capacitor shifts the VIDL level down by  $V_{SW}$ . The swing of VIDH and VIDL is still limited to  $1 \times V_{SW}$ , but the combined voltage range of the display is  $2 \times V_{SW}$ .

In order to make this work, the display circuit must be changed. First, two video input pins must be used instead of only one as before. The extra signal to the display is easily accommodated in the flexible printed circuit. Second, the complementary MOS column drivers are split; the p-channel transistor is connected to VIDH and the n-channel transistor is connected to VIDL. The horizontal scanner circuits must be designed to activate only one transistor of the pair at a time. Finally, dc-restore switches must be added to maintain the desired voltages across the coupling capacitors. Kopin Corp.’s displays that embody the new architecture integrate these switches, so the only additional external components are the capacitors themselves.

Figure 3 incorporates a timing diagram that illustrates ac-coupled operation. The VID signal is kept low at the beginning of the first row, while the dc-restore switch for VIDH is closed briefly to set 0 V across the VIDH coupling capacitor. Pixels A and B are written to white and high black using the p-channel column-drive transistors.

The polarity of VID is inverted before the second row is written, so VID is held at high while the switch to VIDL is closed. This sets the VIDL capacitor voltage to  $V_{SW}$ , but leaves the VIDH capacitor voltage unchanged. The n-channel column drivers are then activated to write pixel C to white and pixel D to the low black level  $-V_{SW}$ . The VID polarity is switched again at the end of the row, in preparation for the dc restore of VIDH.

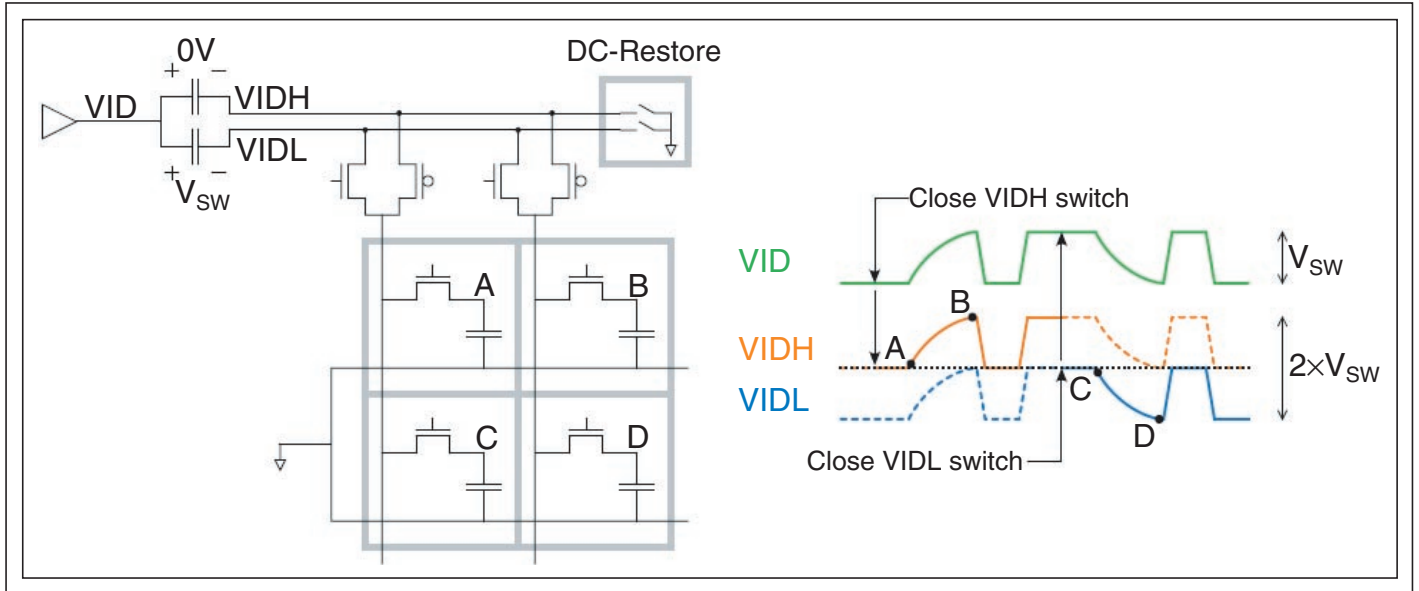
### Display Designs

This low-voltage technique has been used in several commercial-display designs (Table 2). The first two displays in the table are a pair of color and monochrome displays initially developed for viewfinder applications, having demanding cost and size constraints but relatively modest resolution requirements. The color display packs 113,000 dots into a 0.16-in.-diagonal device by using a delta dot arrangement on 6.3- and 11.3- $\mu\text{m}$  horizontal and vertical pitches, respectively. The monochrome version shares the same form

**Table 1: Voltage Swings for the Three Drive Schemes**

	DC-common	AC-common	AC-coupled	
Amplifier output swing	$2\times$	$1\times$	$1\times$	$V_{SW}$
Display video input swing	$2\times$	$1\times$	$2\times$	$V_{SW}$
VCOM swing	0	$1\times$	0	$V_{SW}$
Pixel voltage swing	$2\times$	$3\times$	$2\times$	$V_{SW}$

# display architectures



**Fig. 3:** In the new display architecture, a single amplifier drives the VID signal having a swing of  $1 \times V_{sw}$ . The swing of the VIDH and VIDL signals is still limited to  $1 \times V_{sw}$ , but the combined voltage range presented to the display is  $2 \times V_{sw}$ .

factor, but features  $300 \times 225$  square pixels on an  $11\text{-}\mu\text{m}$  pitch.

A color-stripe pattern is used for the higher-resolution displays, with full-color square pixels made up of  $5 \times 15\text{-}\mu\text{m}$  RGB dots. Commercial products with this pixel design include the quarter-VGA and SVGA displays described in Table 2. Because of its compact  $0.24\text{-in.}$ -diagonal size, the QVGA display is well-suited to lightweight eyewear applications, such as the binocular display modules (BDM) shown in Fig. 4. The BDM subsystem includes the display, backlight, drive electronics, and pre-aligned optics, ready for integration into video eyewear applications. The BDM is manufactured in the same cleanroom as the display itself, minimizing potential dust or particle contamination and thereby relaxing the cleanliness requirement for system assembly.

The block diagram shown in Fig. 5 corresponds to the QVGA display and is also representative of other displays using this architecture. The circuit is powered by VDD and VSS power supplies at  $+3.3$  and  $-5$  V, respectively, but the digital I/O pins use  $3.3\text{-V}$  logic between VDD and VEE =  $0$  V. The VEE power supply also serves as the common electrode to the pixel array and as the reset level to the integrated dc-restore switches.

Most of the digital inputs are level-shifted before entering the control logic, but the complementary pixel clocks CK0 and CK1 pass directly to the data scanners, which are designed to accept  $3.3\text{-V}$  clocks directly. This avoids the need for an internal clock driver, which saves power and minimizes skew between the digital clocks and the analog video. The power needed to drive the display

is less than  $4$  mW, exclusive of backlight.

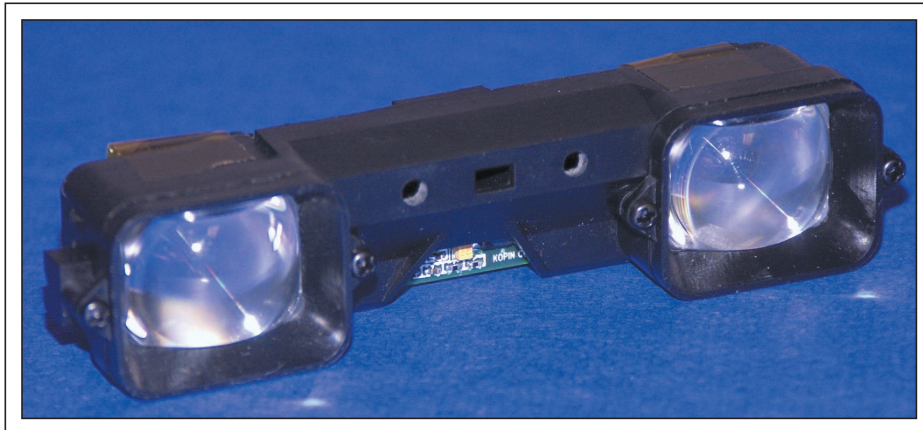
The only other timing signals are the horizontal and vertical start pulses (HS and VS, respectively), and the inversion control signal INV. The INV signal tells the display which set of dc-restore switches to close when HS goes high at the start of the line, and also tells the data scanners whether to activate the n- or p-channel column drivers. Two more pins set the vertical and horizontal scan directions; DWN and RGT are typically wired high or low to suit the optics configuration, but may be switched during operation for applications requiring image rotation. The last input, SLEEP\*, activates the power-control circuits to disable the scanners and write  $0$  V to the entire pixel array. The display may remain powered while in the sleep mode; all other inputs will be ignored. Sleep mode is also activated when a low-voltage condition is detected on VDD or VSS. Finally, output pins TOUT1 and TOUT2 are provided for electrical tests in manufacturing, but these are not used in normal operation.

### Driver ICs

The real benefits of ac-coupled architecture become apparent when designing the driver IC. Of course, an immediate power savings can be expected because the amplifier output swing is reduced from  $2 \times V_{sw}$  to  $1 \times V_{sw}$ . But, more importantly, typical values of  $V_{sw}$

**Table 2: Commercial Displays Using ac-Coupled Architectures**

Display	Diagonal (in.)	Resolution (dots)	Dot Pitch (mm)
113k LV	0.16	$521 \times 218$	$6.3 \times 11.3$
300S	0.16	$300 \times 225$	$11 \times 11$
QVGA	0.24	$3 \times 320 \times 240$	$5 \times 15$
SVGA	0.59	$3 \times 800 \times 600$	$5 \times 15$



Kopin Corp.

**Fig. 4:** Because of its compact 0.24-in.-diagonal size, a QVGA display based on the new architecture is well-suited to lightweight eyewear applications, such as this recent binocular display module.

of about 3.0 or 3.3 V are readily achievable by using rail-to-rail amplifiers in conventional CMOS processes. The resulting CMOS driver ICs can be significantly less expensive than the BiCMOS drivers typically used with

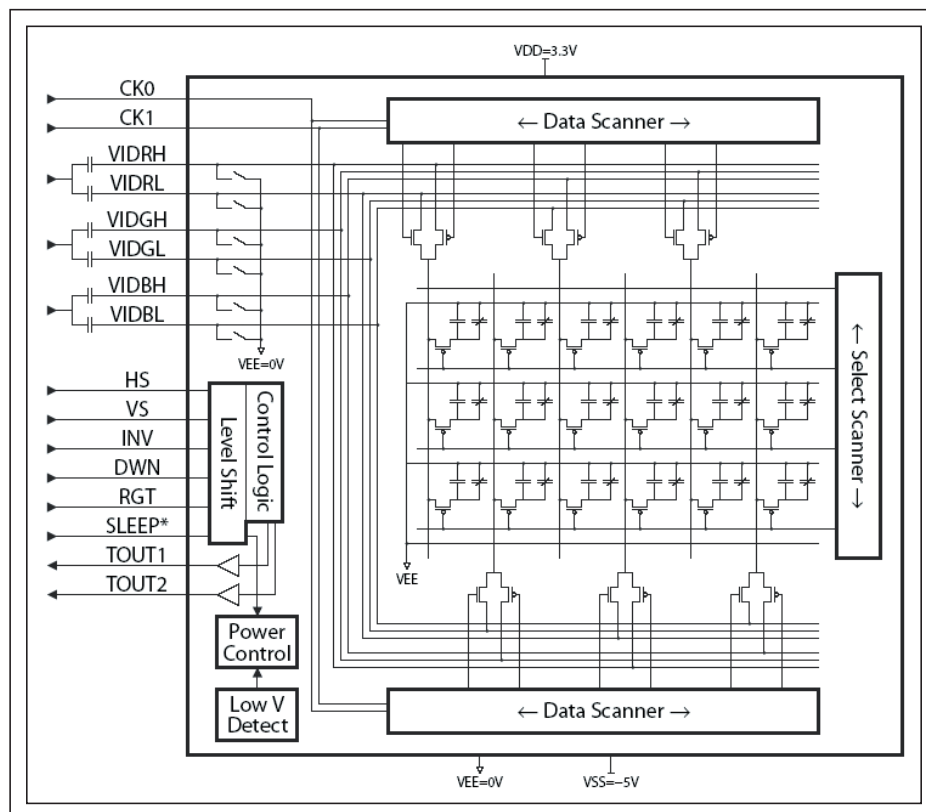
conventional dc- or ac-common display architectures. And finally, the use of a CMOS process affords a higher level of integration, which leads to reductions in system complexity, size, and cost.

The first driver chip to utilize the ac-coupled architecture was built to drive the 300S monochrome display in camcorder viewfinders. The video signal path of the IC is entirely analog, from the SMPTE-170M video input, through the gain and gamma-correction circuits, to the CMOS rail-to-rail video amplifiers. An integrated sync separator and PLL provide a time base for the chip's digital logic, which generates all the required display timing signals.

The monochrome driver became the ancestor of a family of chips, for which many of its blocks can be reused in subsequent designs for both analog and digital and monochrome and color applications.

### Conclusion

The new ac-coupled architecture enables low-power near-to-eye microdisplays to be powered with CMOS-compatible 3.3-V power supplies. The resulting lower power consumption and system cost, combined with a compact form factor, make these displays especially attractive for mobile video applications such as tiny 0.16-in. viewfinders with resolutions of QVGA to SVGA and beyond. This display family is likely to find new uses, such as watching DVDs or digital TV on the go, mobile computing, and playing 3-D video games on lightweight eyewear systems. ■



**Fig. 5:** Shown is a block diagram of the QVGA display.