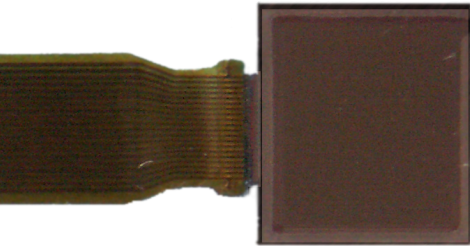
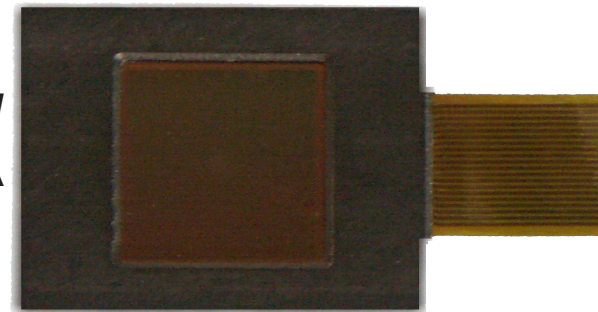


CyberDisplay® VGA

Ultra-Compact Color AMLCD



Frameless
Part No. KCD-VDCF-AA



Framed
Part No. KCD-VDCF-BA

1 GENERAL DESCRIPTION

The CyberDisplay® VGA is a color-filter active matrix liquid crystal display (AMLCD) with a spatial resolution of 640 × 480. The CyberDisplay VGA utilizes high-performance single-crystal silicon transistors, and is the smallest (0.44 inch diagonal) transmissive AMLCD for VGA resolution. The transmissive AMLCD allows the use of simple and thin optics for compact system size.

The CyberDisplay VGA has conventional DC-coupled R,G,B analog inputs. Bidirectional horizontal and vertical scanner circuits are integrated. A sleep mode is provided to facilitate and simplify system power management schemes.

Figure 1-1 shows the pixel array layout. Each square full-color pixel comprises red, green, blue color dots (4.7 × 14.1 μm). The active array of 1920 × 480 dots is surrounded by opaque dummy pixels, for a total size of 1932 × 484 dots.

The CyberDisplay VGA is available in a frameless package (KCD-VDCF-AA) for integration into a viewfinder module or a framed package (KCD-VDCF-BA) for attachment to a snap-on backlight module.

1.1 Applications

The ultra-compact CyberDisplay VGA is ideal for viewfinders for digital cameras or lightweight eyewear for watching movies, sporting events and music videos, browsing the Web and checking e-mail from mobile devices such as cell phones, or playing games on the go.

1.2 Key Specifications

- 640 × 3 × 480 active color dots (VGA resolution)
- 644 × 3 × 484 active color dots
- 4.7 (W) × 14.1 (H) μm dot pitch
- Ultra-compact 0.44"-diagonal
- Active pixel area (9.0 mm x 6.8 mm)
- Parallel RGB analog inputs
- Digital control inputs accept 3.3 and 5.0-volt logic levels
- Power-saving sleep mode
- Integrated horizontal and vertical scanners
- Bidirectional horizontal and vertical scanning

PS-0095 07202006

The display products and systems described herein are covered by numerous issued U.S. and foreign patents and pending applications owned by or licensed to Kopin Corporation. These specifications are subject to change without notice.

2 ELECTRICAL SPECIFICATIONS

A functional block diagram of the CyberDisplay VGA is shown in Figure 2-1. Integrated scanners drive the active matrix pixel array. The horizontal data scanners switch the red, green, and blue video inputs onto the column lines, with timing controlled by complementary clocks HCK1 and HCK2. The vertical scanner selects rows one by one, using a single clock VCK. The RGT and DWN inputs control the horizontal and vertical scan directions; both should be held high for standard left-to-right, top-to-bottom scanning. The row inversion drive scheme requires that video polarity be inverted on alternate lines.

2.1 Interface Signals

A 20-pin flex cable provides electrical connection to the CyberDisplay VGA. The interface signals are listed in Table 2-1.

2.2 Supply and Signal Voltages

Figure 2-2 shows the voltage levels used for typical operation. The CyberDisplay VGA requires three supply voltages: VSS, VCC, and VDD. Most of the display's internal circuits are powered by VDD and VSS, typically 9.5 and 0 V respectively. The interface circuits also use the VCC supply, the voltage of which should be set to the high limit of the digital input swing (3.3 V typ). The VCOM pins are tied to the pixel array's common electrode, a large capacitive load. Although VCOM ideally draws zero current, it does require a low-impedance drive to handle transient currents.

The video inputs swing from the low black level (VLK) to the high black level (VHK), with the white level at video center (VVC).

Pin	Symbol	Description
1	VCOM	Pixel common electrode
2	RSV	Reserved output
3	VIDR	Red video input
4	VIDG	Green video input
5	VIDB	Blue video input
6	HCK1	Horizontal clock
7	HCK2	Horizontal clock
8	HST	Horizontal start
9	RGT	Left-to-right scan
10	DWN	Top-to-bottom scan
11	VCK	Vertical clock
12	VST	Vertical start pulse
13	EN	Row enable
14	SLEEP*	Sleep mode
15	VDD	Supply = +9.5V
16	VCC	Interface supply = +3.3V
17	VSS	Supply = 0V
18	TOUT1	Test output
19	TOUT2	Test output
20	VCOM	Pixel common electrode

* Signal is active low

Table 2-1: Supply and Interface Voltage Levels

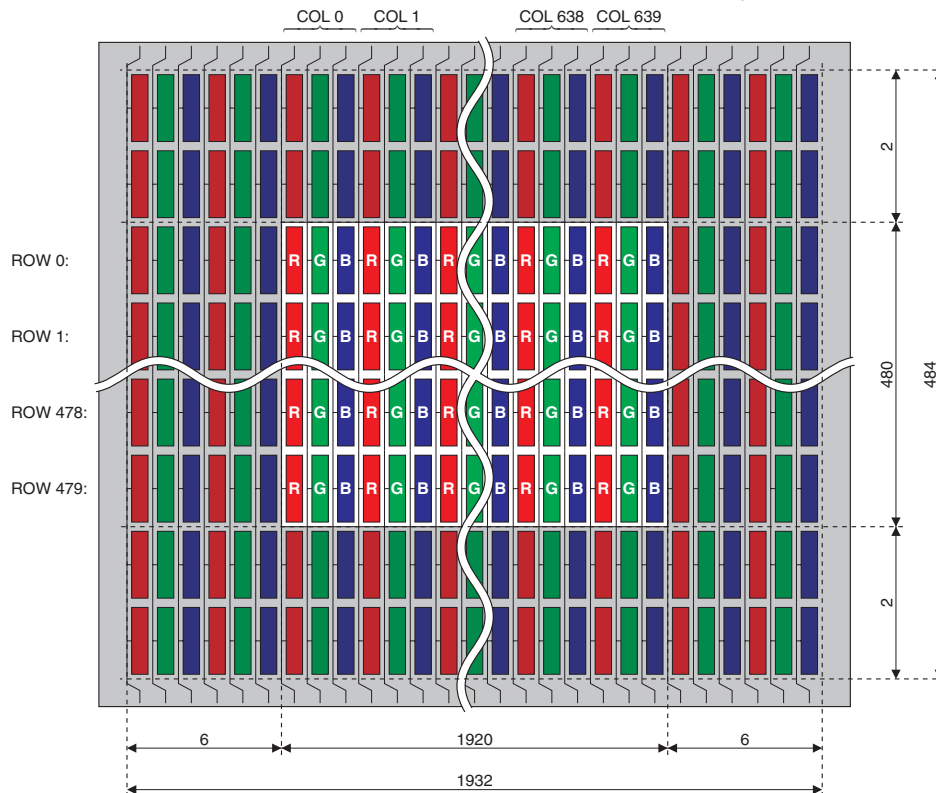


Figure 1-1: Pixel Array

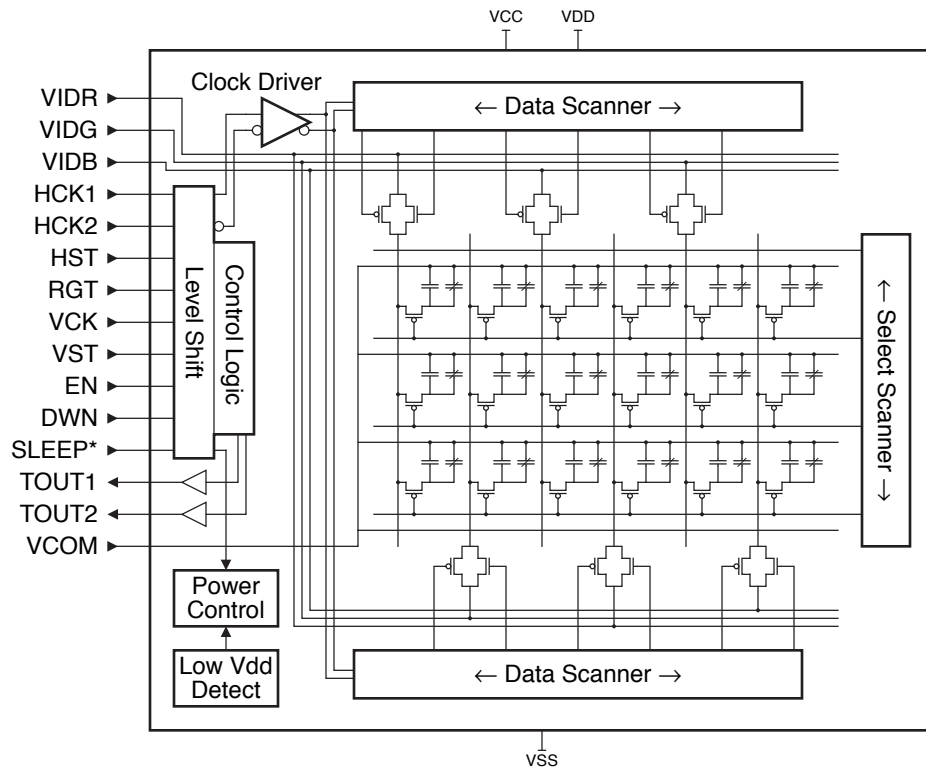


Figure 2-1: Block Diagram

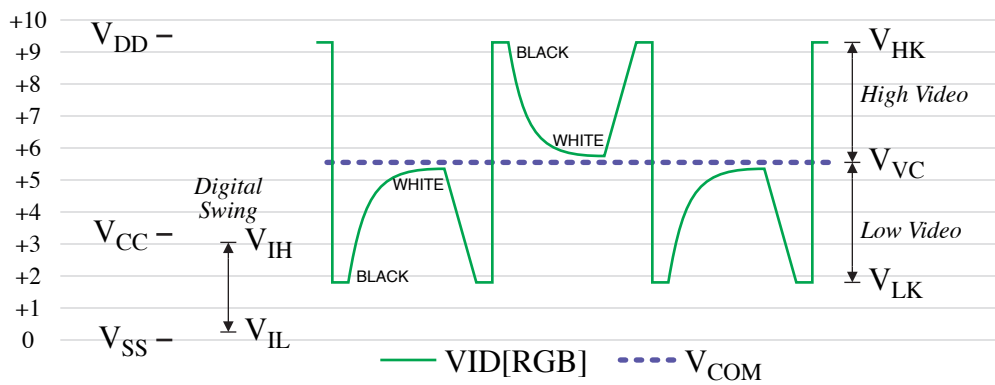


Figure 2-2: Supply and Interface Voltage Levels

2.3 Inversion

To preserve DC balance in the liquid crystal, each pixel must be driven with alternating high and low video. The CyberDisplay VGA uses row inversion, in which all pixels of each row have the same polarity, but successive rows have alternating polarity. The row inversion phase must be inverted with successive frames. For example, if one frame is driven with row 0 low, row 1 high, and row 2 low, then the following frame must have row 0 high, row 1 low, and row 2 high.

2.4 Sleep mode

The CyberDisplay VGA's features a sleep mode to simplify system power management. When the

SLEEP* pin is driven low, all scanners are disabled and the pixel array is driven to the white state. The display will draw minimal current while in sleep mode. The VDD, VCC, and VCOM supplies must be maintained at

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V _{DD}	- 0.5	11	V
Supply voltage	V _{CC}	- 0.5	V _{DD} + 0.5	V
All inputs	V _I	- 0.5	V _{DD} + 0.5	V

Note: All voltages relative to V_{SS}=0.

Table 2-2: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage — internal	V _{DD}	8.2	9.5	9.8	V
Supply voltage — interface	V _{CC}	3	3.3	3.6	V
Operating current — internal	I _{DD}		8.8	10.5	mA
Operating current — interface	I _{CC}				µA
Sleeping current — internal	I _{DDs}		150	550	µA
Sleeping current — interface	I _{CCs}		10		µA
Video high black level	V _{HK}		9.3	V _{DD}	V
Video center level	V _{VC}		5.55		V
Video low black level	V _{LK}		1.8		V
Common electrode voltage	V _{COM}	V _{VC}	5.75	V _{VC} + 0.5	V
VCOM current	I _{VCOM}	-10		10	µA
Digital input high	V _{IH}	0.9 V _{CC}			V
Digital input low	V _{IL}			0.1 V _{CC}	V
SLEEP* input high	V _{IHS}			2	V
SLEEP* input low	V _{ILS}	1			V
Test output high	V _{OH}		0.9 V _{CC}		V
Test output low	V _{OL}		0.1 V _{CC}		V
Input current	I _I	- 10		10	µA
Input capacitance: VIDR/G/B	C _{VID}		100		pF
Input capacitance: digital inputs	C _I		10		pF
VCOM capacitance	C _{VCOM}		4		nF

Note: All voltages relative to V_{SS}=0. Supply currents measured at V_{DD}=9.5V, V_{CC}=3.3V.

Table 2-3: Electrical Characteristics and Recommended DC Operating Conditions

their respective operating voltages. The backlight may be turned off.

The display will also enter sleep mode when the integrated low voltage detect circuit determines that power has been removed.

2.5 Electrical characteristics

Permanent damage to the display may result if the

Absolute Maximum Ratings in Table 2-2 are exceeded. The Absolute Maximum Ratings are not typical operating conditions.

2.6 Timing specification

The timing parameters of Table 2-4 are defined in the timing diagrams in the figures of this section.

Parameter	Symbol	Min	Typ	Max	Units
Frame period	t_V		13.3–16.7		ms
Frame rate	$1/t_V$		60–75		Hz
Line period	t_H		26.7–31.7		μ s
Line frequency	$1/t_H$		31.5–37.5		kHz
Clock period	t_{CP}	62.5	63.5–80		ns
Clock frequency	$1/t_{CP}$		12.5–15.75	16	MHz
Video sampling period	t_{PP}	$(t_{CP}/2)-5$		$(t_{CP}/2)+5$	ns
HCK1–HCK2 clock skew	t_{CSK}	-5		5	ns
HST setup	t_{HS}	20			ns
HST hold	t_{HH}	20			ns
VCK high pulse width	t_{KH}	200			ns
VST setup to VCK	t_{VHS}	100			ns
VST hold after VCK	t_{VHH}	100			ns
VCK to EN delay	t_{KED}	400			ns
EN to VCK delay	t_{EKD}	400			ns
EN to active video delay	t_{EVD}	800			ns
Active video to EN delay	t_{VED}	2.5			μ s
Video setup	t_{VS}	5			ns
Video hold	t_{VH}	15			ns
Test output delay	t_{TD}				ns

Table 2-4: Electrical Characteristics and Recommended AC Operating Conditions

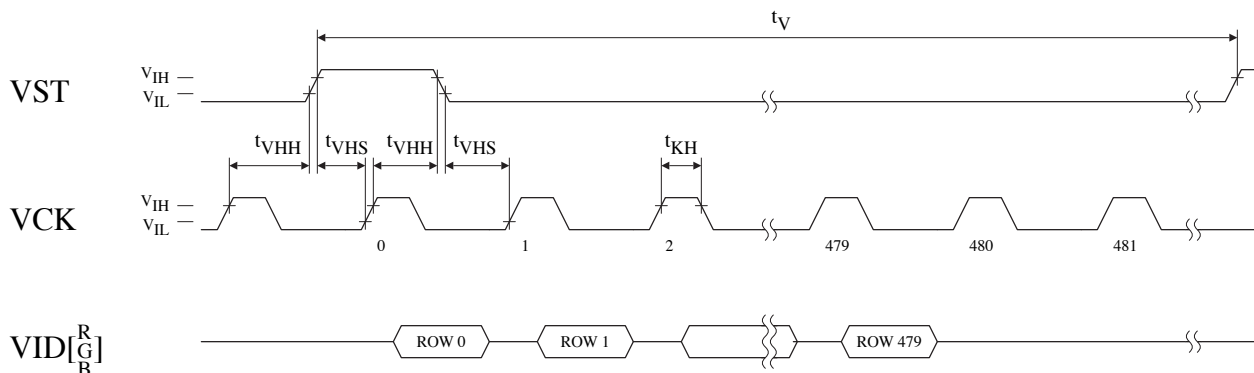


Figure 2-3 Horizontal Timing

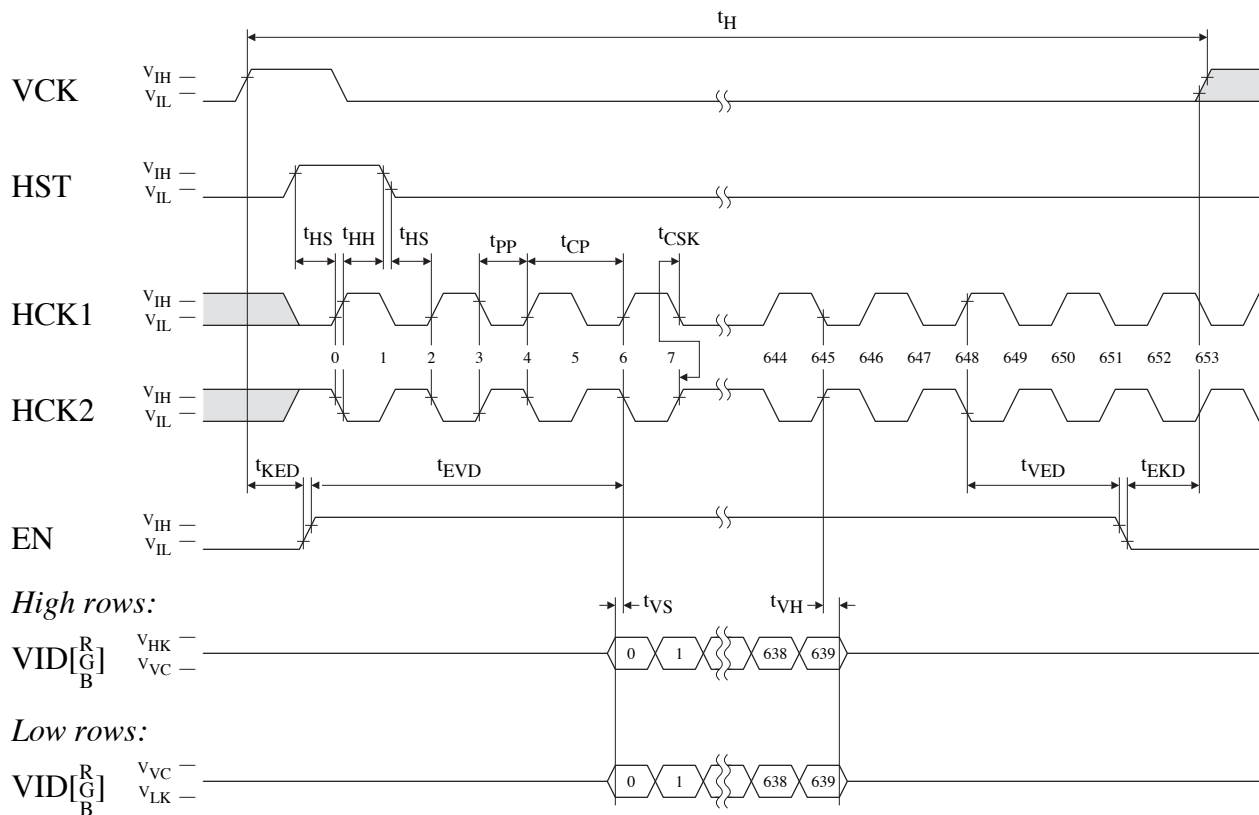


Figure 2-4: Vertical Timing

2.7 Nominal Timing for Typical Applications

The diagrams of this section present nominal timing for several common video modes. The timing is parameterized in terms of S, the horizontal start position. Nominal values of S are given for each format, but it is recommended that S be made configurable in the drive electronics.

2.7.1 480-line formats

Figure 2-5 shows timing for VESA VGA formats up to 75 Hz, and for progressive scan derivatives of the NTSC and PAL video standards. The timing for 480/60p video is based on SMPTE 293M Annex B, with a line frequency twice that of NTSC. (Although SMPTE 293M properly requires a 16:9 aspect ratio, the same timing is also used with 4:3 formats.)

The 576/50p format is based on line-doubled PAL timing. The pixel frequency is set to $786/t_H$ (~12.3 MHz), resulting in a 5:6 pixel aspect ratio. This will produce square pixels after vertical scaling to reduce 576 lines per frame to 480 display lines. In the simplest case, such scaling may be performed by skipping every sixth input line, but more sophisticated algorithms may obtain better results.

2.7.2 240-line formats

Figure 2-6 illustrates 240-line formats for NTSC and PAL. Both formats require 1:2 vertical expansion to

match the display's 480 lines. PAL additionally requires 6:5 vertical scaling, as described above for 576/50p. These deinterlacing and scaling operations are best performed in an external digital signal processor or display driver ASIC. Alternatively, the line doubling and/or skipping drive schemes described below may produce acceptable results in less demanding applications.

Figure 2-7 illustrates the line doubling scheme recommended for displaying 240-line video on the CyberDisplay VGA. The VCK and EN signals are double-pulsed after each row n, thereby copying the video information to row (n+1). Line doubling halves the vertical resolution while continuing to update all pixels at the field rate (50 or 60 Hz).

An alternative method for displaying NTSC or PAL video is to interlace by line skipping, optionally with line doubling. In Figure 2-8, only the even or odd rows are written in each field, while the other rows are skipped. The scheme of Figure 2-9 is similar, but uses line doubling rather than skipping. Each pixel is updated at the field rate, but the polarity inversion frequency is reduced to 12.5 or 15 Hz. In either case, the full 480-line vertical resolution is maintained, but image quality may be degraded. The CyberDisplay VGA scanners support both interlacing modes, but they are not recommended for best image quality.

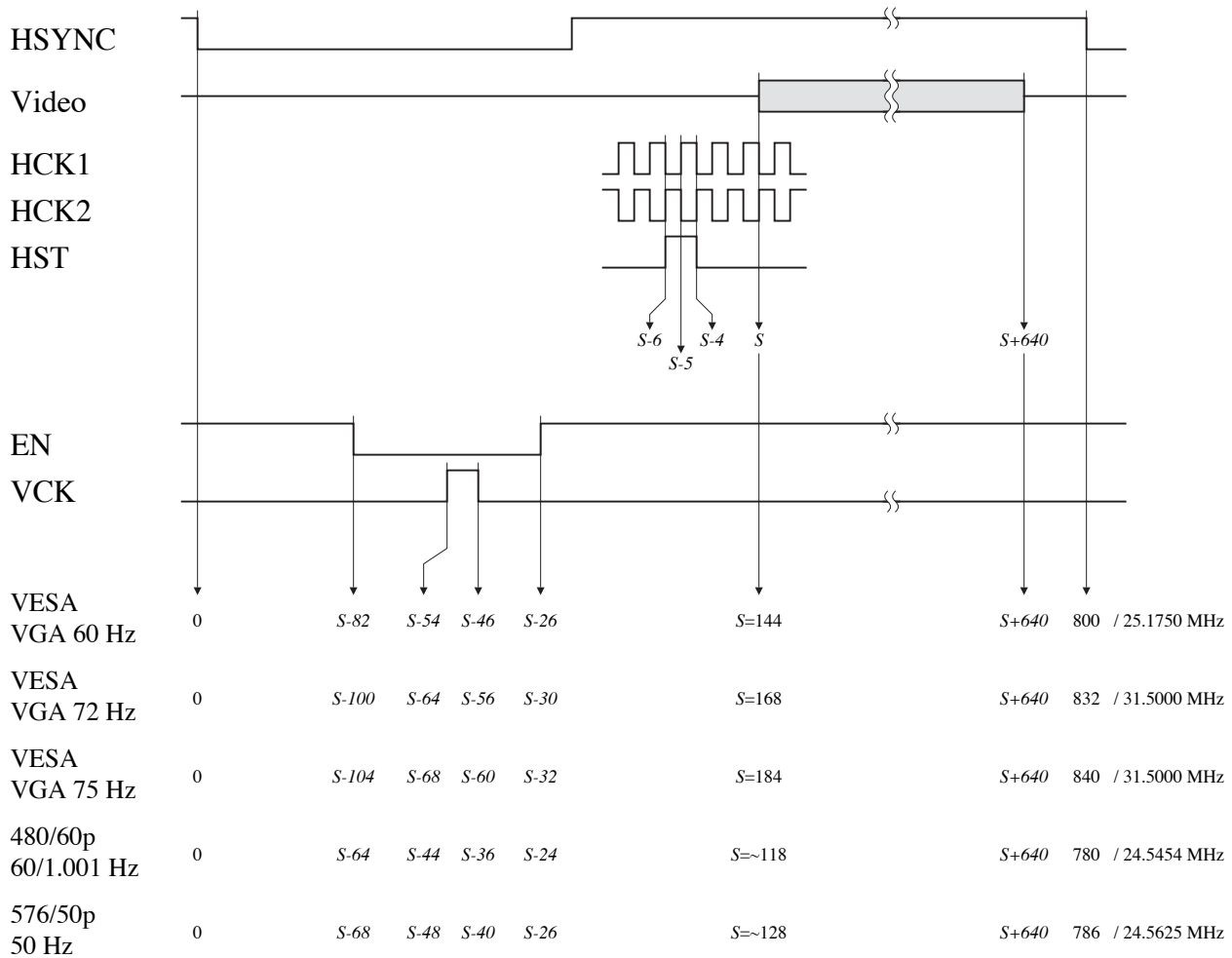


Figure 2-5: Nominal Timing for Selected 480-line Formats

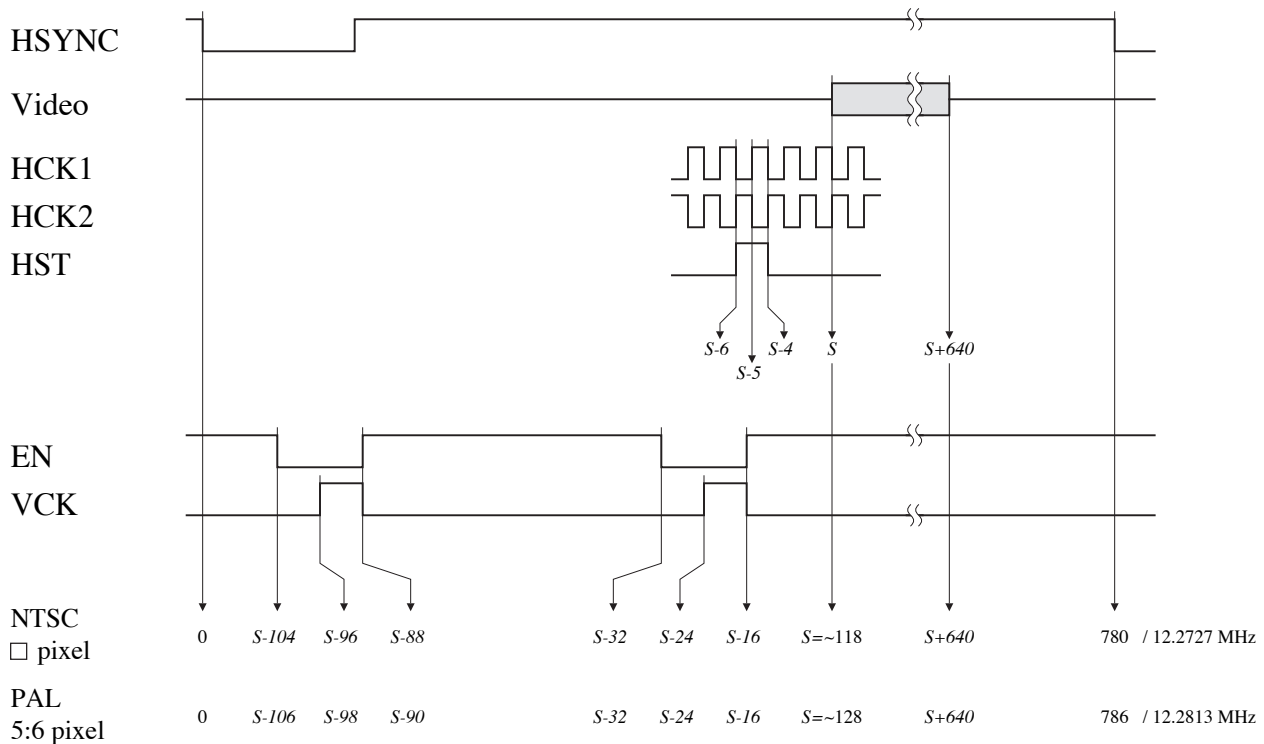


Figure 2-6: Nominal Timing for Selected 240-line Formats

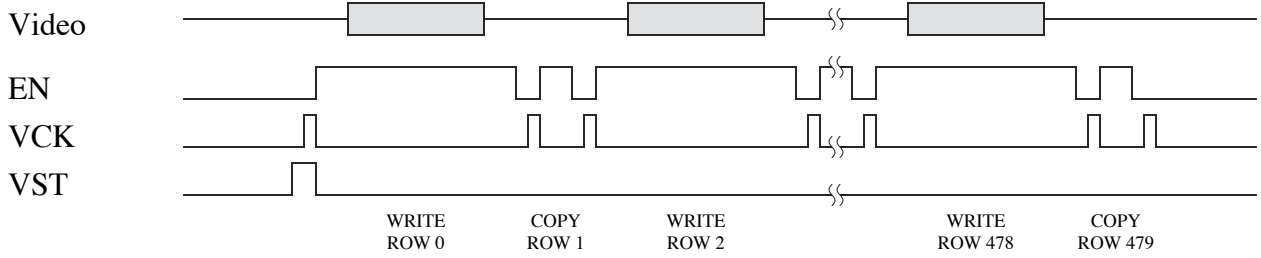
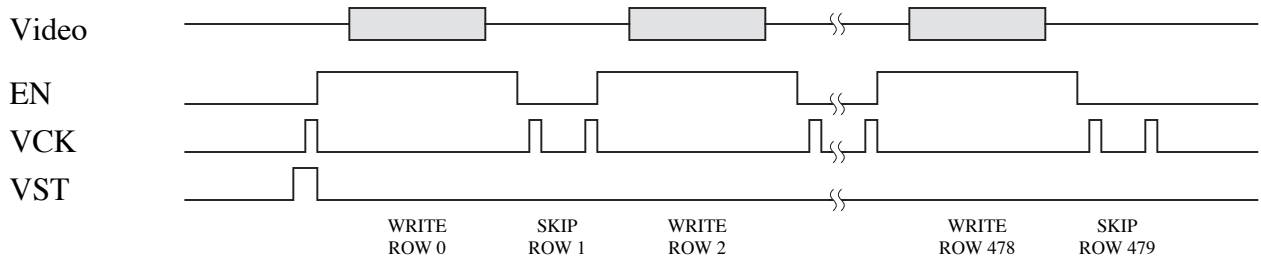


Figure 2-7: Line Doubling

Even rows:



Odd rows:

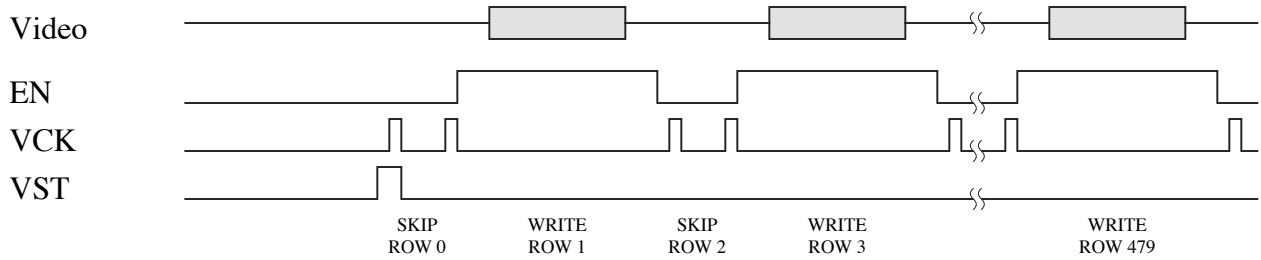
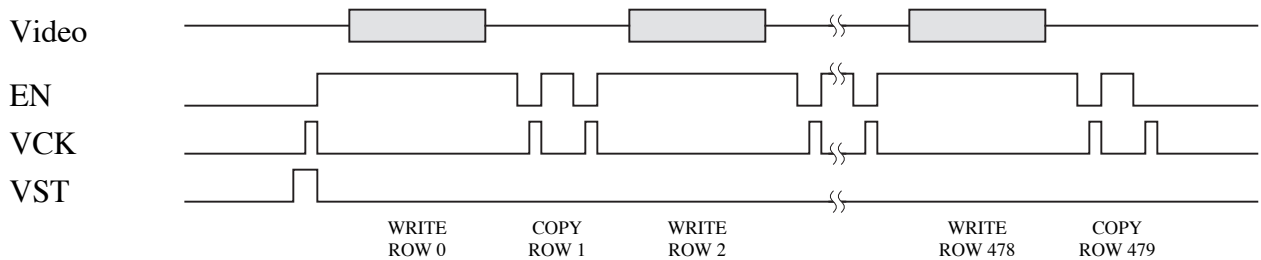


Figure 2-8: Interlaced Scanning with Line Skipping

Even rows:



Odd rows:

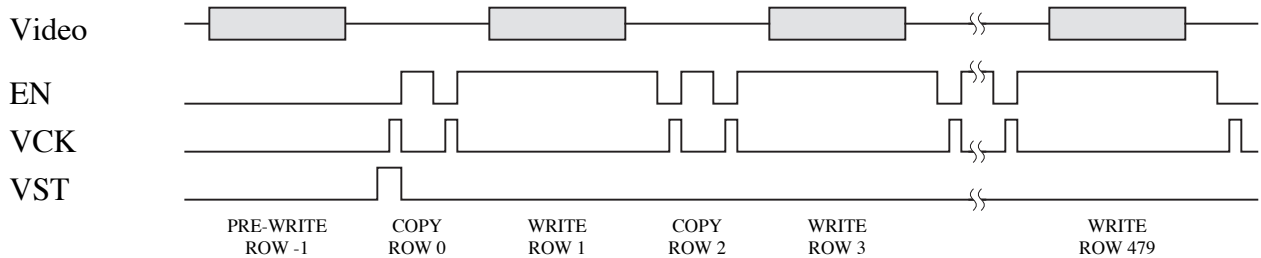


Figure 2-9: Interlaced Scanning with Line Doubling

Row inversion (§2.3) must be performed in the 240-line formats, but it is somewhat more complicated than in the 480-line formats. The rules are:

1. The first line is written with the polarity opposite that of the previous frame. In interlaced modes, one frame equals two fields.

2. Successive lines are written with the polarity opposite the previously written row (skipped or copied lines are not considered).

3 OPTICAL SPECIFICATIONS

3.1 Optical Characteristics

Item		Symbol	Notes	Min	Typ.	Max	Unit	
Contrast ratio	Vsig = 5.55 + 3.75V	CR _{3.75,25}	1	60	80	—	—	
Optical Transmittance	25°C	T	2	1.5	1.7	2	%	
Chromaticity	W	X	3	0.26	0.3	0.34	CIE standards	
		Y						Wy
	R	X						Rx
		Y						Ry
	G	X						Gx
		Y						Gy
	B	X						Bx
		Y						By
V-T characteristics	V ₉₀	25°C	V ₉₀₋₂₅	4	0.4	0.7	1.1	V
	V ₅₀	25°C	V ₅₀₋₂₅					
	V ₁₀	25°C	V ₁₀₋₂₅					
Response time	ON time	25°C	ton ₂₅	5	—	10	20	ms
	OFF time	25°C	toff ₂₅					
Flicker			F	6	—	—	-40	dB
Center Brightness @ If _{LED} = 20 mA	Θ = 0	L	7	120	140	160	cd/m ²	

Table 3-1: Optical Characteristics

Notes On Measurement Conditions:

1. CR_{3.75,25} = (Luminance White)/(Luminance Black). System I
2. T = (Luminance White)/(Luminance Backlight). System I
3. CIE Standard 1931. White backlight: 7500K. System II
4. V-T is relationship of signal amplitude to transmittance. System I
5. 0% to 90% transmittance. System I + Oscilloscope
6. 20log(AC/DC) @ 50% transmittance. System I + Spectrum Analyzer
7. Measured at the center of powered display under proper image condition.

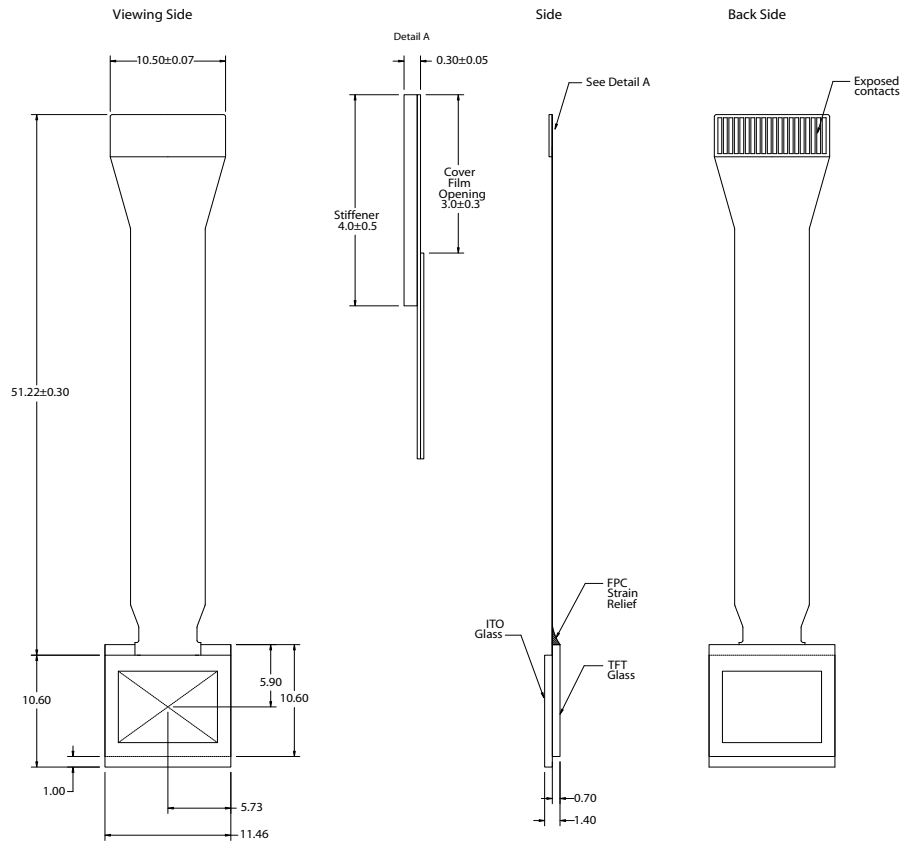


Figure 4-2: CyberDisplay VGA Display (frameless) and FPC Assembly

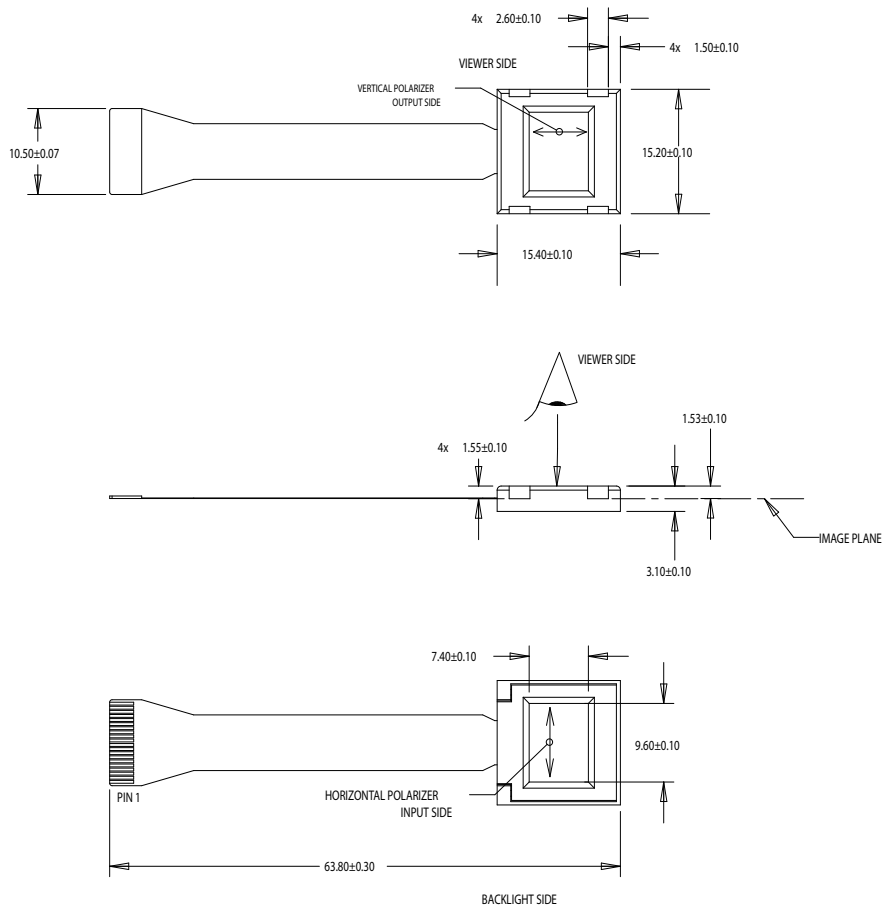


Figure 4-3: CyberDisplay VGA Display (framed) and FPC Assembly